Overview

Today’s emerging markets aren’t playing by yesterday’s rules... design or otherwise. SoC architects developing cutting edge wearable, wireless, augmented reality and IoT devices can no longer make do with standard memory IP to deliver lower and lower power targets. Their designs are ahead of the game. They demand application specific power and performance; targets that demand “out-of-the-box” thinking, targets that deliver market leading energy efficiency.

When they need extraordinary ultra-low power Memory IP they turn to SureFit™, sureCore’s application-centric custom memory design service to deliver on their unique design and PPA requirements. Memory tuned to their low-power needs. Memory tuned to their disruptive innovation. Memories that are designed, validated, characterized and ready to integrate.

SureFit™ applies patented proven design techniques and innovative memory architectures including:

- Segmented arrays and bit line voltage control to deliver optimal dynamic power and performance.
- sureCore SMART-Assist circuitry to deliver robust near-threshold operation across process and temperature extremes.
- Highly granular sleep modes, coupled with independent sub-banks, to put power saving control in the hands of system architects.
- Custom-designed single-port and multi-port bit cells
- Pipelined read circuitry to deliver on demanding performance goals.

Proven Techniques

SureFit™ deploys patented and proven low-power design techniques that prioritize power optimization over speed and area.

Customers come seeking many attributes including multiple read/write ports, ultra-low leakage retention modes, low dynamic power, near-threshold operation, write masking and BIST/DFT support. Memory tuned to their precise requirements. Memory tuned to deliver the target performance demanded by next generation products.

SureFit™ develops memory variants including SRAM and Register Files based on either standard foundry or custom bit cells, the latter capable of delivering ultra-low operating voltages, improved leakage characteristics and improved performance.

Innovative Memory Architectures

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<th>Bit Line Voltage Control &amp; SMART-Assist techniques</th>
<th>Software controllable sleep modes on a per bank basis</th>
<th>Patents granted for optimizations</th>
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Industry Leading Energy Efficiency

| Near threshold voltage operation | >50% dynamic and >20% static power savings |

enquiries@sure-core.com
SureFit’s power saving techniques are process technology agnostic and have been demonstrated in bulk CMOS, FDSOI and FinFET.

The bottom line? Customized ultra-low power memory IP built to your exact specifications that hits dynamic power targets, operates at near-threshold voltages, delivers multiple read/write ports and provides a suite of comprehensive sleep modes that meets challenging leakage targets.

Advanced Verification & Characterisation
A rigorous verification regime incorporating statistical, parametric and physical validation ensures that SureFit™ application-centric memories meet demanding quality requirements. Accurate industry-standard timing and power views are delivered from flows based on leading memory characterization tooling and multiple PVT corners are generated quickly and automatically.

Summary
When your designs are ahead of the game and standard IP no longer delivers, turn to sureCore to develop a memory tuned to your exact needs. Meeting challenging power goals means challenging assumptions - standard IP delivers standard performance. Make your product stand out with sureCore’s SureFit™ application-centric custom SRAM memory design service.

Contact us at enquiries@sure-core.com