surecore

CUSTOMISED LOW POWER SRAM SOLUTIONS

CryoCMOS IP to Unlock Quantum Computing

cryoIP

HIGHLIGHTS

- Specially Engineered CryoCMOS IP
- Characterised down to 4˚K
- Minimal Power Dissipation
- Reduces Thermal Load
- Standard Cell Library Recharacterisation
- IP Portfolio for Cryo-ASIC's
- SRAM, ROM, Register file compilers
- ADCs, DACs & Temp sensors

MARKET APPLICATIONS:

- CryoASIC Design for Quantum Computers
- CryoASIC Design for High Performance Computing

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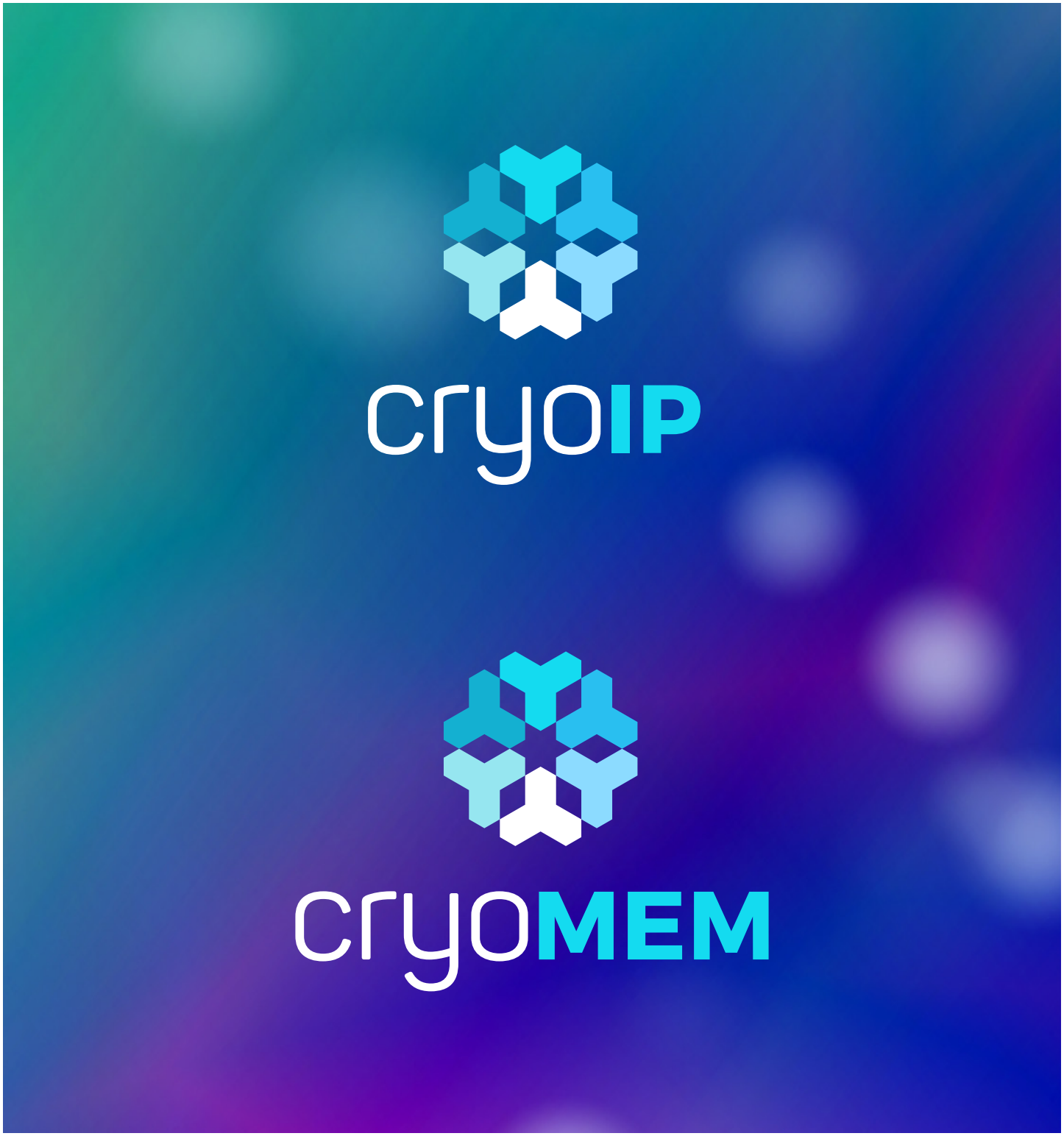
Our range of CryoCMOS IP is suitable for operation at the extremely low temperature required for Quantum Computing (QC) applications. This *CryoIP*™ family will enable the design of CryoCMOS control chips that can be co-located with the qubits in the cryostat. This will help solve the current problem of extensive and performance limiting cabling used to connect the qubits with their associated control electronics usually running at room temperatures outside the cryostat. For Quantum Computers to realise their incredible potential, thousands, if not millions of qubits will be needed, and they must be kept at cryogenic temperatures to ensure correct operation. Currently, the major barrier to scaling is the amount of control cabling, which is in direct proportion to the number of qubits within the system. This problem can only be solved by moving the control electronics into the cryostat.

We are uniquely positioned to solve two of the key challenges to developing CryoCMOS. Currently, the standard industrial operating temperature range for most commercial CMOS process technologies is from -40˚C to 125˚C and this is reflected in the transistor SPICE models supplied by silicon foundries. By working closely with both industry partners and foundries, we plan to design and characterise silicon IP capable of operation down to 4˚K.

The second challenge is to ensure that the control electronics dissipates as little heat as possible so as to minimise the thermal load on the cryostat. Hence it is critical that, as far as is possible, low power design techniques are deployed.

We already have silicon-proven, ultra-low power, embedded memory IP that we will customise for this cryogenic application and will be launched as our *CryoMem*™ range. Using the knowledge gained from the development of *CryoMem*, we plan to create a range of IP tailored for the development of complete QC control electronics in CryoCMOS. The company will offer a complete portfolio of this *CryoIP* for licensing by companies wishing to develop Cryogenic control ASICs.

This new *CryoIP* library will help unlock the potential of QC by accelerating the development of cost effective, cryogenic control ASICs for the hundreds of QC companies out there competing to deliver competitive Quantum Computer solutions.



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