surecore

# Ultra Low Voltage Embedded SRAM
# Product Information

everON

## HIGHLIGHTS

- Wide operating voltage range: 0.6V – 1.2V
- Up to 70% dynamic power saving
- Up to 60% leakage power saving
- Advanced sleep modes on independent banks
- Up to 250MHz performance in 28nm at 0.7V

## TECHNOLOGY

- 40ULP, 28HPC+, 22ULL

## MARKET APPLICATIONS

- IoT – 'fit and forget', low voltage, low standby power
- AI Edge – tightly-coupled memory
- Wearables, Medical – low voltage, ultra-low power

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## OVERVIEW

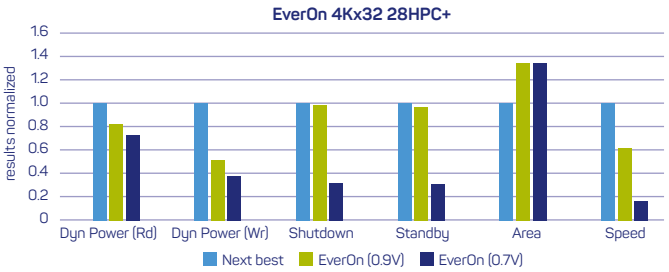
EverOn™ is the 'Always On' solution for 'ultra-low power designs with a wide operating voltage range. EverOn provides read/write access down to the bit cell retention voltage, 0.6V in 40ULP and 22ULL, and 0.63V in 28HPC+ process nodes. It delivers up to 70% dynamic power savings and up to 60% static/leakage power savings compared to foundry and other SRAM solutions.

sureCore provides best-in-class power savings by augmenting standard foundry memory 6T bit cells with its innovative, patented architecture, powerful compiler technology and a set of finely grained sleep modes.

Product development includes the implementation and execution of a comprehensive verification and characterization strategy.

Detailed datasheets spell out power, performance and timing data covering all process corners across a wide operating voltage range. The full industrial temperature range of -40C to 125C is supported.

### EverOn – Enabling the Near-Threshold Revolution




## PRODUCT FEATURES

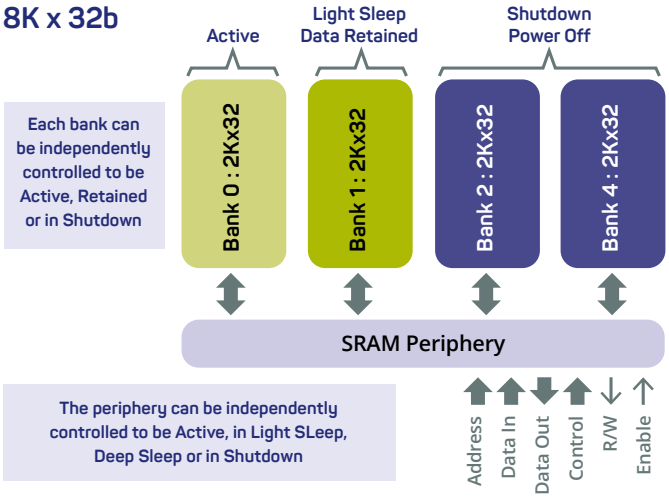
EverOn™ is designed with a rich set of innovative features and functions that contribute to significant power savings.

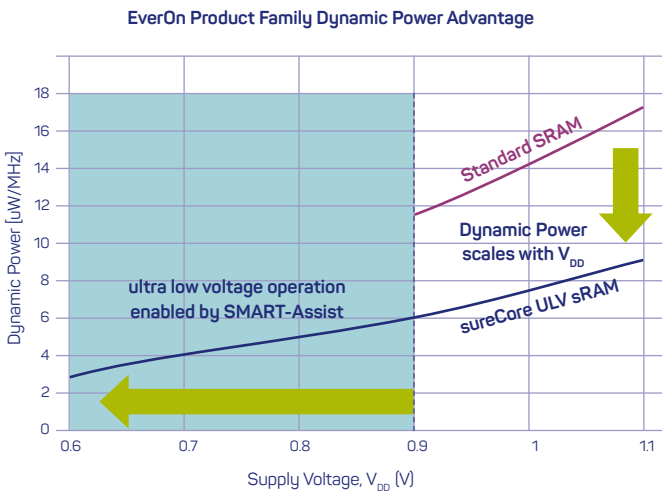
- Single port, single voltage rail synchronous SRAM
- Hierarchical Bit Line Architecture – sub-diving the array into columns/ rows, banks and local blocks
- 'Smart Assist' – controls voltage drive to selected bit cells and bit lines in read and write cycles
- Pre-charge mux sense – read circuit that helps reduce both active and leakage power in the memory array
- SVT Periphery – enables higher performance at low operating voltages
- Configurable global data mux sets column length and overall aspect ratio
- Programmable sleep modes: Light Sleep, Deep Sleep (data retention), Shutdown, configurable on an individual bank basis, up to 4 banks supported
- Configurable word length from 16 to 72-bits
- 576Kbit max instance size. Configurable – 8KX72, 16Kx36
- APTG and BIST support
- Supports industry standard EDA design flows
- Operating voltage down to the bit cell retention voltage

## ADVANCED SLEEP MODES

EverOn comes complete with a rich set of user-programmable sleep modes. Each SRAM is divided into four banks, all independently controllable as either active, sleep (retained) or off. This allows one or more memory banks to be shut down, creating additional power savings without splitting one large memory into several smaller instances. In addition, the periphery can be placed into low power mode to achieve even lower power consumption.

**Take a look at this configuration:**




## RIGOROUS VERIFICATION

sureCore's extremely rigorous verification strategy includes silicon validation, high sigma statistical analysis, and identifying and analysing key design parametrics. This supplements a qualification regime that includes an industry-standard 125˚C, 1,000-hour High Temperature Operating Life (HTOL) test that, to date, every device has passed!

Statistical analysis covers PVT extremes with readability, writability and access disturb margins validated at 6σ. An extensive Monte Carlo simulation of specific design parameters, validated across the full PVT space, assures robust operation. A thorough physical verification suite including IR drop, EM and crosstalk checks augment this regime.

This strategy covers the full compiler design space, accounting for both global and local variability effects, delivering robust designs that achieve high yields in production.

## SRAM CHARACTERISATION STRATEGY

sureCore has invested heavily in leading edge tooling that builds an extensive and automated SRAM characterization environment that accurately determines all timing arcs across a full range of operating corners. This is key to achieving outstanding EDA model accuracy.

## COMPILER SUPPORT

sureCore's SRAM technology was built specifically for scalable memories. Because EverOn's low power and low voltage operation doesn't require detailed tuning, its suitable for memories with many different capacities and word lengths. sureCore's memory compiler supports capacities from 4Kbit to 576Kbit and provides a tool for both the rapid estimation of power, area, and performance as well as generating fully characterised memory instances. sureCore memories easily integrate into typical SoC design flows through compiler generated industry-standard simulation, layout, timing analysis and DFT views.

## SUMMARY

sureCore's innovations are an industry step change, delivering dramatically improved power consumption with limited area overhead. EverOn provides system architects with a range of new trade-offs previously not possible with existing designs.



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