surecore

LOW POWER MEMORY SOLUTIONS

MiniMiser™ delivers dramatic power savings for computationally intensive portable applications

miniMISER

HIGHLIGHTS

- Custom Register File Architecture
- Power savings >50%
- Wide operating voltage range
- Tuneable performance
  – Ultra Low Voltage
  – High speed operation
- Single rail – interfaces directly to logic
- Supports multiple read/write ports

MARKET APPLICATIONS:

- Next Generation Earbuds
- Intelligent Hearing Aids
- Intense Edge AI Solutions
- Health Trackers

SUPPORTED NODES:

- TSMC 28HPC+, 22ULL, 16FFC, 12FFC
- GF 22FDX, 12LP+

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MiniMiser™ is a tuneable multi-port register file architecture that can support both low power and high-performance applications. Its unique implementation reduces power consumption by over 50% and gives developers a new way of optimising the power envelope for their design. By swapping off-the-shelf register files with MiniMiser significant power savings can be realised. By reviewing the application's operational demands designers can further enhance this by introducing multiple performance modes tied to various operating voltages thereby ensuring the SoC is tuned to application need. As MiniMiser is not based on the foundry bit cell its single rail design means it can be directly connected to the system logic without the usual design headaches such as level shifters and static timing analysis challenges.

As wearable devices integrate increasing AI capabilities to enrich the user experience and provide product differentiation, ever more memory will be needed to support the computing demands driving up the overall power budget. Cutting and optimising power usage is critical to extending recharge windows and delivering a competitive product. As part of the system logic needed to deliver the computational capability register files are ubiquitous small blocks of memory providing either interim storage for calculations or interfacing between blocks in different clock domains. Typically, more efficient than flip-flop based register storage the standard bit cell based implementation is performance limited when developers look to move outside the typical operating norms. Multiple read/write ports, wide operating voltages and extremely high performance needs often drive designers back to power hungry flip-flops. MiniMiser elegantly addresses these challenges with dramatic power and area savings.

As previously outlined, standard off-the-shelf Register File IP is usually based on the foundry bit cell, and whilst this gives optimal area utilisation, the power metrics are often poor – with the bit cell itself precluding a reduction in operating voltage to tune the logic for a range of performance goals. Designers are forced to implement multiple power islands – at least one for the logic and one for the memories. This introduces a level of physical design complexity plus the addition of level shifters as well as necessitating considerable care with the timing analysis strategy. The MiniMiser architecture readily supports both a wide operating voltage range as well as the capability to deliver the high performance needed by AI and other computationally intensive applications.

The MiniMiser architecture is based on a customised storage element and exploits sureCore's SRAM power saving techniques to deliver significantly improved power characteristics even at nominal process voltages. The architecture lends itself to several optimisation criteria – multi-port and high-performance variants can be readily generated by the company's powerful proprietary compiler technology. As MiniMiser is not based on the foundry bit cell then its yield characteristics, like the logic, follow the process d0 thereby easing DFT considerations.

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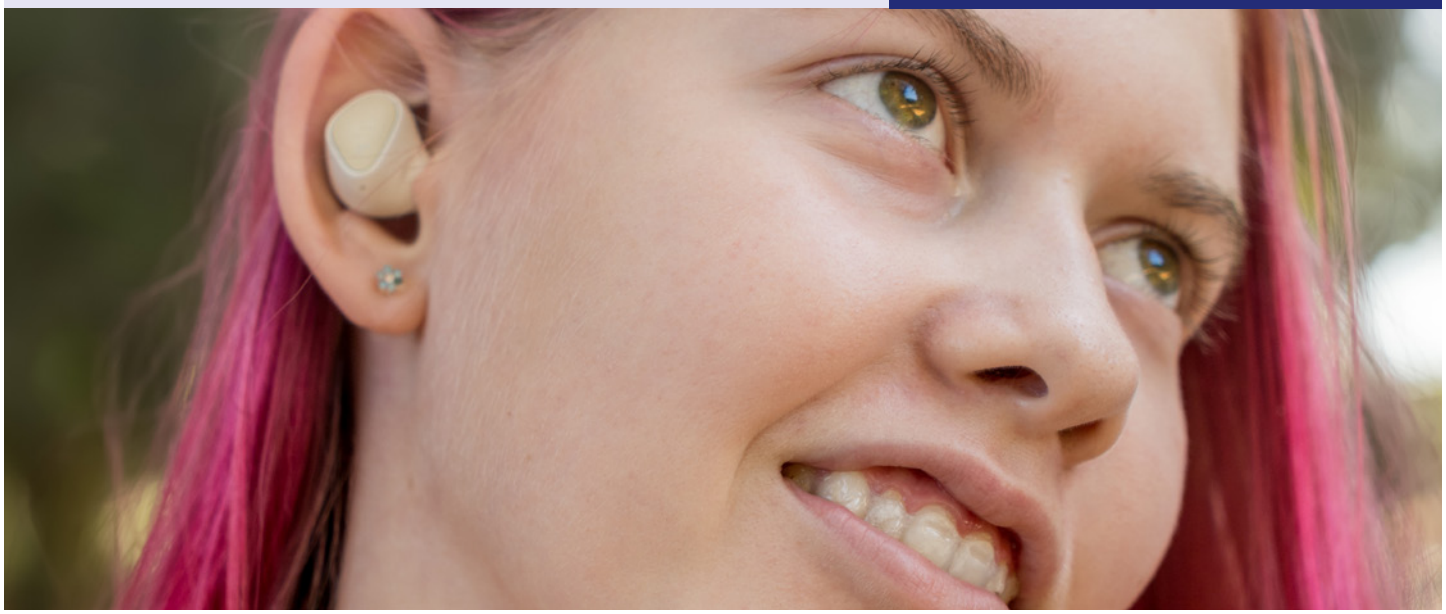

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